

17.7 A 160×128 Single-Photon Image Sensor with On-Pixel 55ps 10b Time-to-Digital Converter

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Image sensors capable of resolving the time-of-arrival (ToA) of individual photons with high resolution are needed in several applications, such as fluorescence lifetime imaging microscopy (FLIM), Förster resonance energy transfer (FRET), optical ranging, and positron emission tomography. In FRET, for example, typical fluorescence lifetime is of the order of 100 to 300ps, thus deep-subnanosecond resolutions are needed in the instrument response function (IRF). This in turn requires new time-resolved image sensors with better time resolution, increased throughput, and lower costs. Solid-state avalanche photodiodes operated in Geiger-mode, or single-photon avalanche diodes (SPADs), have existed for decades [1] but only recently have SPADs been integrated in CMOS. However, as array sizes have grown, the readout bottleneck has also become evident, leading to hybrid designs or more integration and more parallelism on-chip [2,3]. This trend has accelerated with the introduction of SPAD devices in deep-submicron CMOS, that have enabled the design of massively parallel arrays where the entire photon detection and ToA circuitry is integrated on-pixel [4,5].

In this paper, we present an array of 160×128 pixels capable of detecting the ToA of single photons, implemented in 0.13μm CMOS technology. The block diagram of the system is shown in Fig. 17.7.1. The sensor is partitioned into 4 identical quadrants that are served by a balanced clock tree so as to minimize skews and to ensure the fastest possible readout process. The pixels in the rows are read out in rolling shutter mode in two directions (top and bottom) simultaneously. The 10b content of each pixel is thus transferred to the exterior of the chip via 320 independent serializers, 2 for each column, working in parallel at a maximum rate of 160Mb/s, thus enabling in principle the readout of a complete frame in 4μs. In our implementation the frame rate is actually lower, due to current limitations in the readout firmware. The region-of-interest (RoI) is programmable, via vertical and horizontal registers that select which rows and columns are read out.

The pixel is shown in Fig. 17.7.2a; it comprises a SPAD, implemented as a p+/p-well/deep n-well junction, a TDC based on the architecture reported in [5], and a memory. The TDC is composed of a ring oscillator (RO) with fast start-up, shown in Fig. 17.7.2b, that is activated by the SPAD through falling signal *R* and a ripple-counter that is incremented upon each completion of a ring cycle via *B*₃. The ripple-counter, chosen for its compactness and simplicity, provides the 7 most significant bits of the measurement, for a coarse resolution of 440ps. The 3 least significant bits are provided by the eight intermediate RO outputs. These signals are a thermometer code representing the partial propagation of the circulating signal within the RO; they are transferred via control signal *T*, latched, and converted to a binary code (*D*₀: *D*₂), all within the pixel, as shown in Fig. 17.7.2c. The STOP is provided by *S*, freezing the ring oscillator, while a rising *R* resets the TDC (RO and counter). The overall resolution of the TDC is 55ps, its full scale is 55ns. The RO is a replica of a similar one implemented in a PLL outside the pixel array; the ROs are bound by global signal *V*_{PLL} that ensures that the propagation time of a cycle is constant and independent of PVT variations without the need to stop measurements for calibration as in [2]. Due to the negligible fixed-pattern noise measured on chip, pixel-to-pixel variability needs not be compensated.

The pixel supports both time-correlated single-photon counting (TCSPC) and time-uncorrelated photon counting (TUPC) modes. TUPC is achieved by direct counting; the dead time of the SPAD was chosen so as to keep afterpulsing at a reasonable value. In TCSPC mode, a ToA measurement is available in each pixel every 100ns. However, due to measurement sparsity, it is reasonable to retain only one of ten measurements in a minimum frame time of 1μs. Thanks to the

use of the pixel-level memory, readout dead time is suppressed, while reverse START-STOP ensures that only those ROs are active that are in a measurement phase; this reduces power consumption, supply ripple, and substrate noise. An I²C module controls all of the chip's state.

The total number of transistors integrated in the chip is 60 million. A pixel pitch of 50μm was selected as a tradeoff between the functionality and optics feasibility. A microlens array was added as a post-processing step to improve the effective fill factor. The sensor was tested in 3 steps, at SPAD, TDC, and system levels. The SPAD performance is reported in the table of Fig. 17.7.6 for specific values of excess bias voltage *V*_e. The TDCs were characterized separately for jitter and nonlinearities. The performance is also reported in Fig. 17.7.6. At system level, the sensor was tested in TUPC mode to compute the DCR distribution over the chip and in TCSPC mode to measure the jitter distribution and its stability in temperature and supply voltage. The test was conducted in the intended photon-starved regime and with higher illumination levels, so as to determine the limits of operation within the specified accuracy. The chip's overall performance was characterized in a PCB-based system based on a dual FPGA Xilinx IV chip-set.

In Fig. 17.7.3a, the median DCR is plotted as a function of excess bias voltage and temperature, while the inset reports the DCR cumulative probability at room temperature for 0.73V excess bias. Figure 17.7.3b shows the measured DNL and INL over the whole range of 55ns. The results of the TCSPC experiment are shown in Fig. 17.7.4a and b, where the IRF is plotted for two laser source wavelengths. In the insets, the FWHM jitter is plotted for different values of excess bias. The laser sources (Advanced Laser Diode Systems, Germany) are pulsed at 40MHz, emitting blue (405nm) and red (637nm) beams with a pulse width (FWHM) of 40ps and 80ps, respectively. Figure 17.7.4c shows the FWHM jitter as a function of incoming light intensity. The plot shows that, when operating in medium exposure the jitter performance is negligibly degraded with respect to a photon-starved regime. Note that in all TCSPC experiments the power of the laser was adjusted so as to minimize pile-up distortion.

The sensor was mounted on a microscope (BX51IW, Olympus, Japan). In TCSPC mode, the blue laser source was used at an average optical power of 2mW. The sample, a Bisaccate Pine pollen grain (Carolina Biological Supply Company, NC, USA) was illuminated through a microscope objective (50×, 0.80 NA, MPlanFL N, Olympus, Japan) via a standard dichroic beam splitter and a 1× adapter lens. The reflected beam was redirected to the sensor via the beam splitter and filters. In TUPC mode, the illumination was a uniform collimated light source obtained from a standard broadband mercury lamp. The sample was stained using a 2-dye system, Harris hematoxylin and phloxinein, with different decay times. Figure 17.7.5a shows the structure of the pollen; Fig. 17.7.5b and c show the resulting intensity and FLIM images and scales, respectively. The FLIM color code corresponds to a decay time estimated using double exponential fit on 300,000 measurements per pixel; Fig. 17.7.5d shows the optical setup used in the experiments. Figure 17.7.6 summarizes the performance of the chip.

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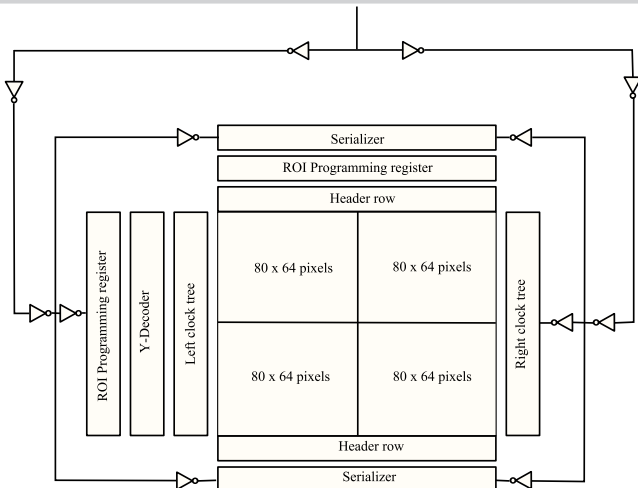


Figure 17.7.1: Block diagram of the sensor, split into 4 identical quadrants. Each pixel is read out in rolling shutter mode towards the top and the bottom simultaneously, with a balanced clock tree minimizing skews. The ROI-programming registers are used for selective row and column readout.

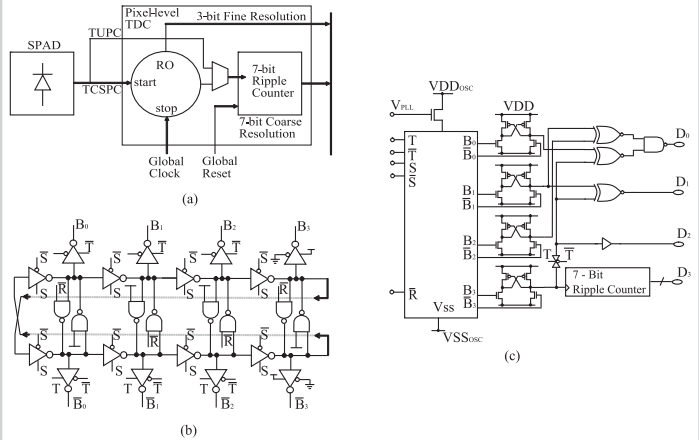


Figure 17.7.2: (a) Pixel schematic: the output of the SPAD acts as a start signal for a ring oscillator (RO) stopped by a global clock. (b) RO schematic. (c) TDC schematic: the frozen RO state is latched, converted from thermometer to binary code, and combined with the coarse measurement.

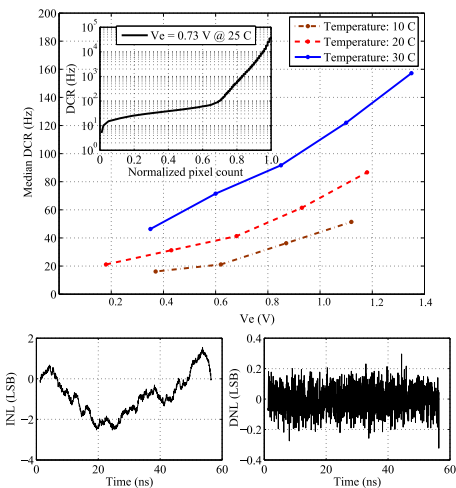


Figure 17.7.3: (a) Median dark count rate (DCR) as a function of excess bias voltage and temperature. In the inset the DCR cumulative probability is shown at 0.73V of excess bias. (b) Worst-case INL and DNL measured over the complete range of 55ns.

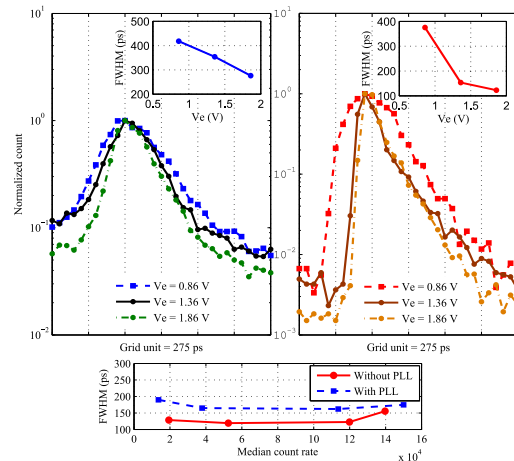


Figure 17.7.4: (a)-(b) Time-domain IRF at two wavelengths: 405nm (a), 637nm (b). In the insets, FWHM jitter as a function of excess bias voltage. (c) FWHM jitter as a function of incident photon flux with various levels of sensor activation, both with and without activating the PLL.

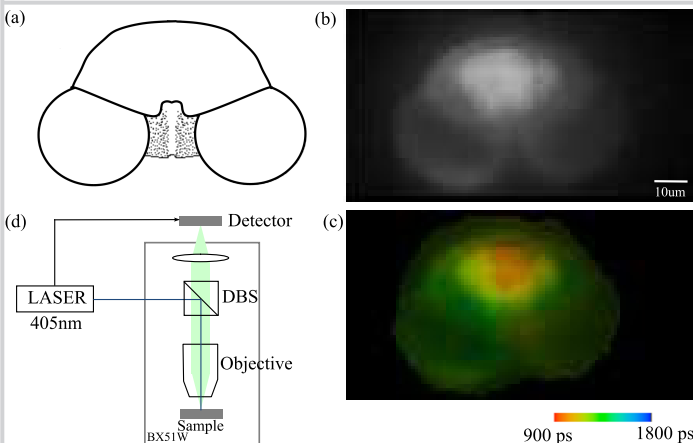


Figure 17.7.5: (a) Structure of a Pine Bisaccate pollen grain [6]. (b) Intensity image of the pollen grain obtained with a microscope with 50x magnification, 1x adapter lens and broadband illumination. (c) Reflection FLIM images of the same pollen obtained with 300,000 frames in 12s. The inset shows the time scale in ps. (d) Microscope setup comprising a 405nm laser source, a dichroic beam splitter, an objective, and the sensor mounted on a C-mount.

Parameter	Condition	Min.	Typ.	Max.	Unit
Pixel	Photon detection probability	$V_e=0.62V$	3	19	%
	Photon detection probability	$V_e=1.40V$	3	27.5	%
	Sensitivity spectrum		350	900	nm
	Dead time			100	ns
	TDC measurement range			55	ns
	TDC resolution (1 LSB)			55	ps
	Measurement rate			1	MS/s
	TDC DNL / INL			$\pm 0.3/\pm 2$	LSB
	Nominal fill factor			1	%
	System	Clock frequency		16	32
Chips size				11.0x12.3	mm ²
Total I/O bandwidth				51.2	Gbps
Power dissipation				550	mW
CMOS Process				130nm	-
FLIM Experiment	Median DCR	$V_e=0.73V$		50	Hz
	Mean FWHM jitter	$\lambda=637nm$		140	ps
	IQ jitter non-uniformity	$\lambda=637nm$, PLL on, count rate = 50kHz		27	ps
	Number of measurements per pixel			3×10^4	-
	Frame rate			25	50
FLIM Experiment	Laser source average power			2	mW
	Average count rate per pixel			15	ke/s
	Target area			125x50	μm^2

Figure 17.7.6: Performance summary for the image sensor. All the parameters were measured at room temperature.

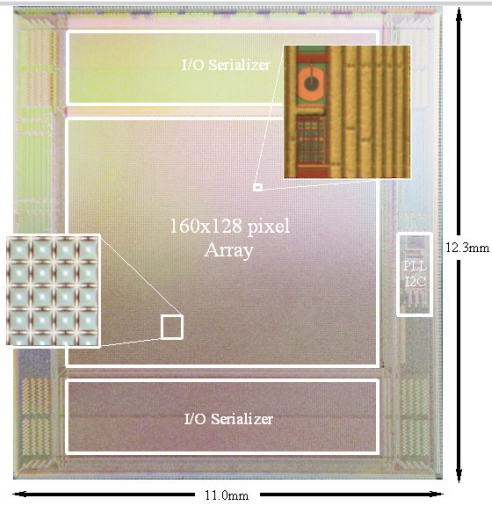


Figure 17.7.7: Photomicrograph of the sensor chip with pixel and microlens array details in the insets. The circuit, fabricated in 0.13 μm CMOS technology, has an area of 11.0 \times 12.3mm². The pixel pitch is 50 μm .